



Contestant number:

Delivery time:

Number of points complex project:

Connection design max. 10b:

Resolution max. 10b:

Display of the max. 10b:

Documentation, max. 10b:

A complex project in the field of electronics

In this part, your task is to design and implement an electronic circuit based on the specified requirements and parameters. The goal is to test the ability to understand the task, the ability to combine theoretical and practical knowledge and the creativity of the contestants.

Do all sketches and calculations directly in the text of the assignment, you have dedicated pages for that. Results without calculation, justification and without correct physical units will not be recognized.

The use of any external assistance is prohibited at the competition. Violation of the regulation will be penalized by disqualification.

Assignment:

Design a circuit, which will measure the frequency of the supplied signal and display it in a human-readable form. The required circuit parameters are:

1. The input signal has the following characteristics:
 - a. rectangular shape with 50% offset
 - b. CMOS logic levels (0/5 V)
 - c. maximum frequency 1000 Hz
2. The frequency must be measured with a resolution of at least 100 Hz, optimally 1 Hz
3. The measured data must be updated regularly, at least once every 5 seconds
4. The measured data must be displayed in a human-readable form (e.g. number, code, reading on a voltmeter, etc.)
5. Supply voltage of the circuit +5 V from an external source
6. You can only use components from the list on the other side of the sheet in the circuit
7. You have one auxiliary signal with a frequency between 1 Hz to 32768 Hz (choose the value) from an external generator, CMOS logic levels, 50% duty cycle

The design of the circuit connection, the complexity and the way the frequency will be measured and the data displayed is entirely up to you.

Document the circuit in detail. Describe the measurement method in detail. Explain why you chose this connection and describe the function of the circuit. Calculate or justify the values of all components. Draw a complete circuit diagram. The diagram must contain all used components, specific values of all components, designation of terminal numbers, etc.

Make the connection on the contact field.

During work, you have the opportunity to continuously test the connection and possibly fine-tune its parameters to achieve the maximum number of points.

The grading is as follows:

1. General design proposal 10 points



2. Basic resolution 100 Hz (2 orders) 5 points, increased measurement resolution 1 Hz (4 orders) 10 points
3. Value display: as a number in the decimal system without the need to convert to Hz 10 points, as a number with the need to convert to Hz 7 points, indication in binary form 5 points
4. Project documentation 10 points

List of material available to you:

Integrated circuits:

| | |
|-------------|--|
| NE555P | Universal timer, astable, monostable circuit |
| MCP6002-E/P | Dual, rail to rail operational amplifier, 1MHz, power supply 1.8 to 5.5V |
| NE5532P | Dual operational amplifier, 10MHz, supply ± 5 to ± 15 V |
| SN74HC00N | NAND 2 inputs, 4 gates |
| SN74HC02N | NOR 2 inputs, 4 gates |
| SN74HC04N | inverter, 6 gates |
| SN74HC08N | AND 2 inputs, 4 gates |
| CD74HC4002E | NOR 4 inputs, 2 gates |
| SN74HC20N | NAND 4 inputs, 2 gates |
| CD74HC21E | AND 4 inputs, 2 gates |
| SN74HC42N | Decoder from BCD to 1 of 10 |
| CD74HCT73E | JK flip-flop, 2 channels |
| SN74HC74N | Flip-flop D, with Set-Reset function, 2 channels |
| CD74HCT93E | 4bit binary counter |
| CD74HC123E | Monostable multivibrator, 2 channels |
| SN74HC138N | 3 bit to 1 of 8 decoder/demultiplexer |
| SN74HC139N | Decoder/demultiplexer 2 bits on 1 of 4 lines. 2 channels |
| SN74LS192N | Synchronous 4-bit BCD decade counter up/down with setting |
| 74HC193N | 4-bit binary up/down counter with setting |
| CD4518BE | 4-bit decade BCD counter |
| CD4543BE | BCD code decoder for 7-segment display with register |

Discrete components:

| | |
|--------------|--|
| BC557A | Transistor PNP bipolar. 50V/100mA/500mW |
| BC547A | Transistor NPN bipolar. 50V/100mA/500mW |
| 1N4148-TAP | Positive signal diode 100V/300mA |
| LTL2R3KRD-EM | LED 5mm red. Operating current 2mA |
| LTL2R3KGD-EM | LED 5mm green. Operating current 2mA |
| TDSR1360 | 7-segment common cathode LED display. Operating current 1mA (!) |

Passive components:

E12 series resistors , tolerance 1%, values 10 Ω to 10 M Ω
capacitors : 1n, 2n2, 4n7, 10n, 22n, 47n, 100n, tolerance typically $\pm 10\%$
ceramic: 220n, 470n, tolerance typically -80...+22%
electrolytic: 1 μ F, 2.2 μ F, 4.7 μ F, 10 μ F, 22 μ F, 47 μ F, tolerance typically $\pm 20\%$
electrolytic: 100 μ F, 220 μ F, tolerance typically $\pm 20\%$

Data sheets for semiconductor components and documentation for integrated circuits can be found on the USB stick you received.

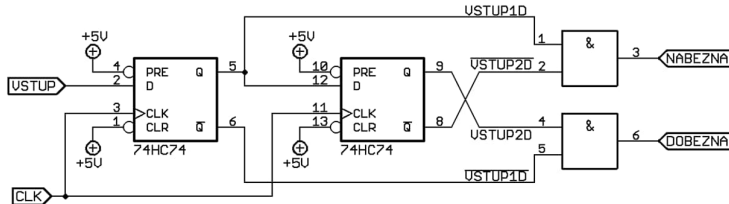
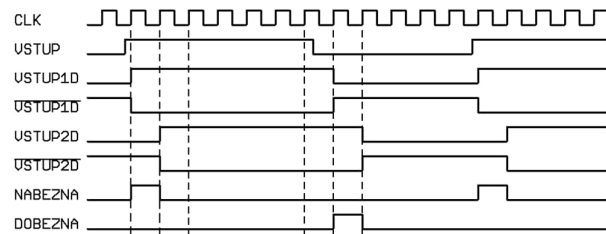


Useful circuits.

For inspiration, we remind you of several connections that may come in handy when developing a circuit diagram according to the assignment.

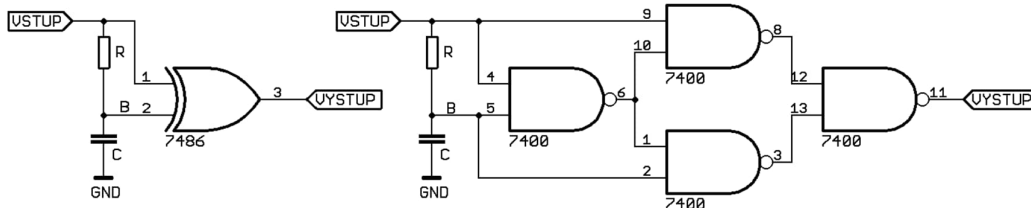
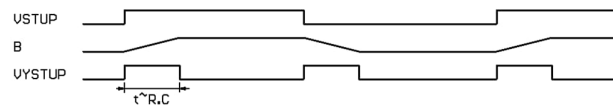
Leading and trailing edge detector

The circuit generates a pulse with the length of one period of the input clock signal on the rising or falling edge of the input pulse.



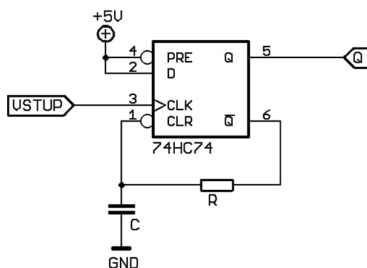
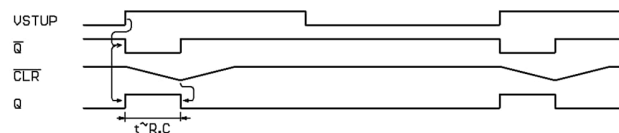
Edge detector

A circuit based on an XOR gate generates a pulse on both the rising and falling edges of the input signal. Also shown is the implementation of the logic function XOR (left) using NAND gates (right). Reasonable pulse lengths are more than a microsecond and significantly less than the duration of the input signal.



Short pulse generator

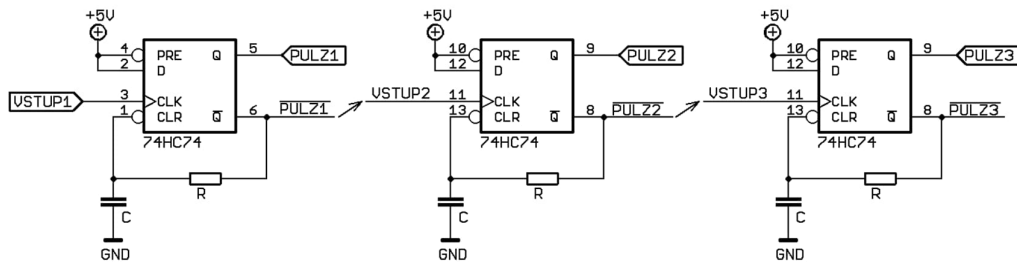
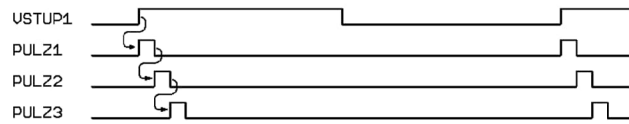
The circuit generates a short 0-1-0 pulse on the rising edge of the input signal. The pulse length is approximately $t \sim RC$. Reasonable pulse lengths are more than a microsecond and significantly less than the duration of the input signal.





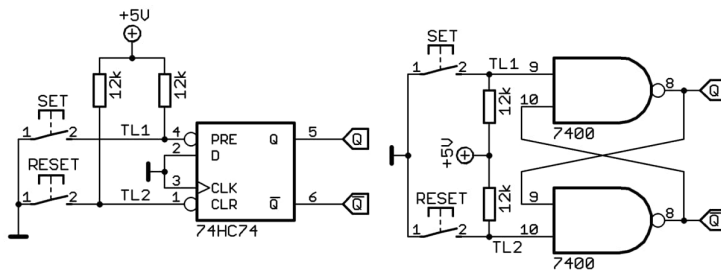
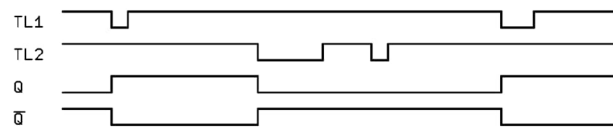
Generator of a series of short pulses

The circuit is based on the connection from the previous point, it uses several chained generators of short pulses. The rising edge of the VSTUP1 signal generates a short pulse PULZ1. This starts the next generator and generates a delayed short pulse PULZ2. In this way, it is possible to generate an arbitrarily long series of pulses, which can be useful for timing, or sequential triggering of events in a more complex circuit. Reasonable pulse lengths are more than a microsecond and significantly less than the duration of the input signal.



RS (set-reset) flip-flop

The RS circuit is a bistable flip-flop circuit that allows memorizing the state, for example, after the arrival of a pulse. It is very often used together with buttons. One button (e.g. Set) is set, the other button (e.g. Reset) is deleted. The picture shows the implementation using the 7474 integrated circuit or the 7400 gates. Both circuits have the same function.





Results

Contestant number:

1. Describe the measurement method in detail. Explain why you have chosen this method/circuit.
2. Describe the function of the circuit.
3. Calculate or justify the values of the components used.

Detailed list of parts and material used:



Complete circuit diagram, including all component values and IC pin descriptions: